EAST SEARCH

10/16/04

L#	Hits	Search String	Databases
L1	20776	register and port and allocat$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	3201	register same (port and allocat$5)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	929	2 and (instruction same (parallel$5 and processor))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	877	register same (port and allocat$5 and instruction and parallel$5 and processor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	699	register same (port and allocat$5 and instruction and parallel$5 and processor)	USPAT; EPO; JPO; DERWENT; IBM_TDB
L6	139	5 and (port near5 shar$5)	USPAT; EPO; JPO; DERWENT; IBM_TDB

Results of search set L6:

US 6801997 B2	Multiple-thread processor with single-thread interface shared among threads	20041005	712/229
US 6735690 B1	Specifying different type generalized event and action pair in a processor	20040511	712/244
US 6694347 B2	Switching method in a multi-threaded processor	20040217	718/108
US 6691301 B2	System, method and article of manufacture for signal constructs in a programming language capable of programming hardware architectures	20040210	717/114
US 6691240 B1	System and method of implementing variabe length delay instructions, which prevents overlapping lifetime information or values in efficient way	20040210	713/400
US 6651222 B2	Automatic design of VLIW processors	20031118	716/1
US 6629312 B1	Programmatic synthesis of a machine description for retargeting a compiler	20030930	717/136
US 6629187 B1	Cache memory controlled by system address properties	20030930	711/3
US 6609163 B1	Multi-channel serial port with programmable features	20030819	710/21
US 6594728 B1	Cache memory with dual-way arrays and multiplexed parallel output	20030715	711/127
US 6581187 B2	Automatic design of VLIW processors	20030617	716/1
US 6542991 B1	Multiple-thread processor with single-thread interface shared among threads	20030401	712/228
US 6507947 B1	Programmatic synthesis of processor element arrays	20030114	717/160
US 6507862 B1	Switching method in a multi-threaded processor	20030114	718/107
US 6499123 B1	Method and apparatus for debugging an integrated circuit	20021224	714/724
US 6496940 B1	Multiple processor system with standby sparing	20021217	714/4
US 6457173 B1	Automatic design of VLIW instruction formats	20020924	717/149
US 6408428 B1	Automated design of processor systems using feedback from internal measurements of candidate systems	20020618	716/17
US 6408375 B2	System and method for register renaming	20020618	712/23
US 6385757 B1	Auto design of VLIW processors	20020507	716/1

US 6351808 B1	Vertically and horizontally threaded processor with multidimensional storage for storing thread data	20020226	712/228
US 6333938 B1	Method and system for extracting control information from packetized data received by a communications interface device	20011225	370/503
US 6311261 B1	Apparatus and method for improving superscalar processors	20011030	712/23
US 6282583 B1	Method and apparatus for memory access in a matrix processor computer	20010828	709/400
US 6275920 B1	Mesh connected computed	20010814	712/14
US 6272617 B1	System and method for register renaming	20010807	712/23
US 6233702 B1	Self-checked, lock step processor pairs	20010515	714/48
US 6216200 B1	Address queue	20010410	711/100
US 6212629 B1	Method and apparatus for executing string instructions	20010403	712/241
US 6212628 B1	Mesh connected computer	20010403	712/226
US 6205223 B1	Input data format autodetection systems and methods	20010320	380/42
US 6195676 B1	Method and apparatus for user side scheduling in a multiprocessor operating system program that implements distributive scheduling of processes	20010227	718/107
US 6179489 B1	Devices, methods, systems and software products for coordination of computer main microprocessor and second microprocessor coupled thereto	20010130	718/102
US 6173388 B1	Directly accessing local memories of array processors for improved real-time corner turning processing	20010109	712/22
US 6161208 A	Storage subsystem including an error correcting cache and means for performing memory to memory transfers	20001212	714/764
US 6157967 A	Method of data communication flow control in a data processing system using busy/ready commands	20001205	710/19
US 6151689 A	Detecting and isolating errors occurring in data communication in a multiple processor system	20001121	714/49
US 6148391 A	System for simultaneously accessing one or more stack elements by multiple functional units using real stack addresses	20001114	712/202
US 6138231 A	System and method for register renaming	20001024	712/216
US 6112019 A	Distributed instruction queue	20000829	712/214
US 6085275 A	Data processing system and method thereof	20000704	710/316
US 6081852 A	Packet data transferring system for autonomously operating a DMA by autonomous boot mode select signal wherein the DMA is enabled to at least one program control list	20000627	710/24
US 6081783 A	Dual processor digital audio decoder with shared memory data transfer and task partitioning for decompressing compressed audio data, and systems and methods using the same	20000627	704/500
US 6065107 A	System for restoring register data in a pipelined data processing system using latch feedback assemblies	20000516	712/32
US 6052773 A	DPGA-coupled microprocessors	20000418	712/43
US 6044451 A	VLIW processor with write control unit for allowing less write buses than functional units	20000328	712/24

US 6012135 A	Computer having multiple address ports, each having logical address translation with base and limit memory management	20000104	711/208
US 6006286 A	System for controlling data packet transfers by associating plurality of data packet transfer control instructions in packet control list including plurality of related logical functions	19991221	710/22
US 5996032 A	System for writing a plurality of data bits less than from the total number of bits in a data register using a single register write operation	19991130	710/62
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US 5964835 A	Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source	19991012	709/216
US 5963746 A	Fully distributed processing memory element	19991005	712/20
US 5963745 A	APAP I/O programmable router	19991005	712/13
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US 5867501 A	Encoding for communicating data and commands	19990202	370/474
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US 5838904 A	Random number generating apparatus for an interface unit of a carrier sense with multiple access and collision detect (CSMA/CD) ethernet data network	19981117	709/250
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